

10-16GHz Low Noise Amplifier

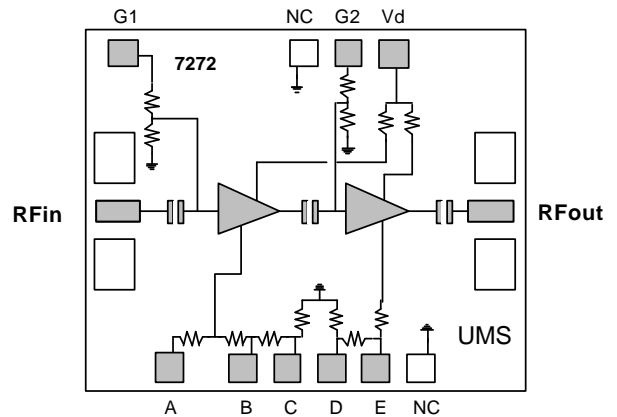
GaAs Monolithic Microwave IC

Description

The CHA2066 is a two-stage wide band monolithic low noise amplifier.

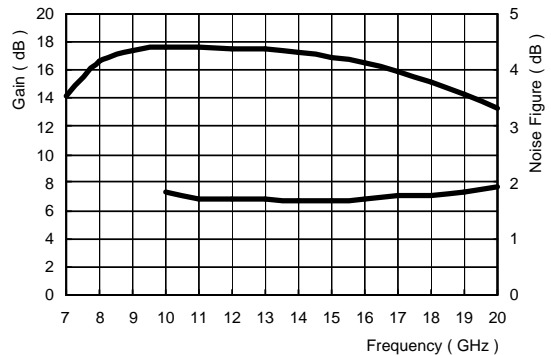
The circuit is manufactured with a standard HEMT process : 0.25 μ m gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is supplied in chip form.



Main Features

- | Broad band performance 10-16GHz
- | 2.0dB noise figure, 10-16GHz
- | 16dB gain, ± 0.5 dB gain flatness
- | Low DC power consumption, 50mA
- | 20dBm 3rd order intercept point
- | Chip size : 1,52 x 1,08 x 0.1mm



On wafer typical measurements.

Main Characteristics

Tamb = +25°C

| Symbol | Parameter | Min | Typ | Max | Unit |
|------------|------------------------|-----|-----------|-----------|------|
| NF | Noise figure, 10-16GHz | | 2.0 | 2.5 | dB |
| G | Gain | 14 | 16 | | dB |
| Δ G | Gain flatness | | ± 0.5 | ± 1.0 | dB |

ESD Protections : Electrostatic discharge sensitive device observe handling precautions !

Electrical Characteristics

Tamb = +25°C, Vd = +4V

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---------|--------------------------------------|-----------------|-----|-------|-------|------|
| Fop | Operating frequency range | | 10 | | 16 | Ghz |
| G | Gain (1) | | 14 | 16 | | dB |
| ΔG | Gain flatness (1) | | | ± 0.5 | ± 1.0 | dB |
| NF | Noise figure (1) | | | 2.0 | 2.5 | dB |
| VSWRin | Input VSWR (1) | | | | 3.0:1 | |
| VSWRout | Ouput VSWR (1) | | | | 3.0:1 | |
| IP3 | 3rd order intercept point | | | 20 | | dBm |
| P1dB | Output power at 1dB gain compression | | | 10 | | dBm |
| Id | Drain bias current (2) | | | 45 | | mA |

(1) These values are representative of on-wafer measurements that are made without bonding wires at the RF ports. When the chip is attached with typical 0.3nH input and output bonding wires, the indicated parameter values should be improved.

(2) This current is the typical value from the low noise low consumption biasing (B & D grounded).

Absolute Maximum Ratings (1)

Tamb = +25°C

| Symbol | Parameter (1) | Values | Unit |
|--------|----------------------------------------|-------------|------|
| Vd | Drain bias voltage (3) | 4.5 | V |
| Pin | Maximum peak input power overdrive (2) | +15 | dBm |
| Top | Operating temperature range | -40 to +85 | °C |
| Tstg | Storage temperature range | -55 to +125 | °C |

(1) Operation of this device above anyone of these paramaters may cause permanent damage.

(2) Duration < 1s.

(3) For a typical biasing circuit : B & D grounded. See chip biasing option page 7/8.

Typical Results

Chip Typical Response (On wafer Sij) :

Tamb = +25°C

Vd = 4.0V ; Vg1 = Vg2 = +1.4Volt ; Id = 45mA (A,B,C,D & E not connected)

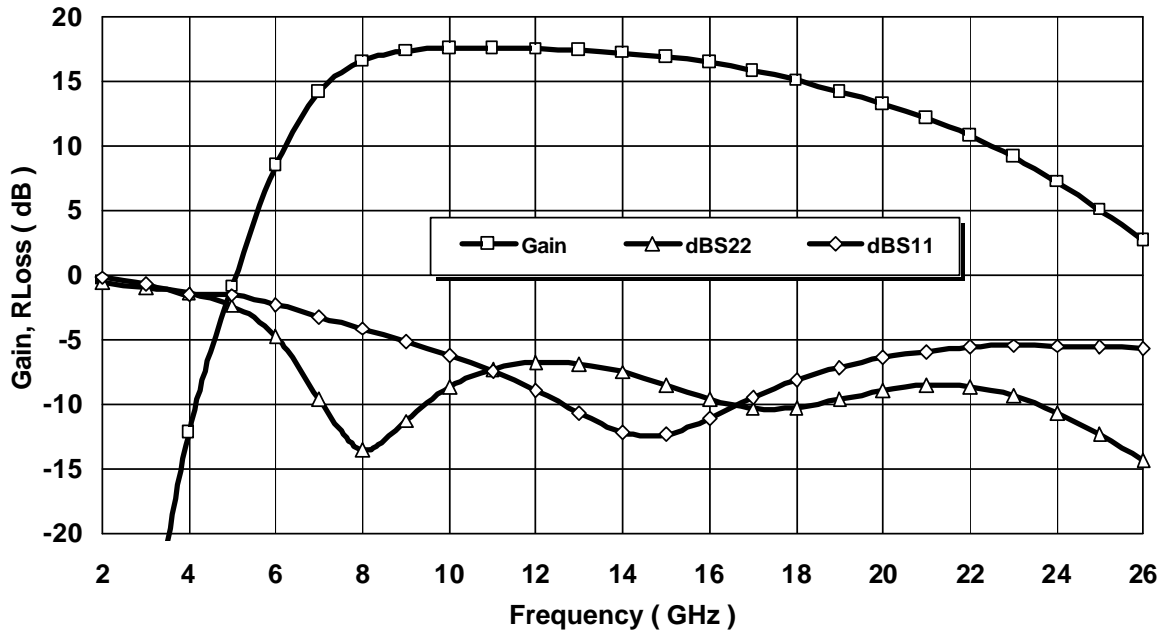
| Freq GHz | MS11 dB | PS11 ° | MS12 dB | PS12 ° | MS21 dB | PS21 ° | MS22 dB | PS22 ° |
|-------------|------------|-----------|------------|-----------|------------|-----------|------------|-----------|
| 1.00 | -0.25 | -16.1 | -82.22 | 90.1 | -46.86 | -148.0 | -0.07 | -7.1 |
| 2.00 | -0.54 | -31.8 | -83.38 | 37.9 | -46.99 | -169.6 | -0.15 | -14.8 |
| 3.00 | -0.88 | -48.8 | -84.02 | 17.8 | -30.57 | -13.6 | -0.67 | -24.3 |
| 4.00 | -1.38 | -68.9 | -72.90 | 21.7 | -12.70 | -58.0 | -1.41 | -26.7 |
| 5.00 | -2.32 | -95.1 | -62.06 | 8.4 | -1.44 | -96.2 | -1.47 | -33.3 |
| 6.00 | -4.51 | -131.2 | -52.22 | -25.9 | 7.98 | -145.4 | -2.17 | -41.3 |
| 7.00 | -8.90 | -177.3 | -45.23 | -71.4 | 13.83 | 154.7 | -3.17 | -46.2 |
| 8.00 | -12.32 | 122.2 | -41.37 | -112.2 | 16.32 | 100.4 | -4.01 | -50.1 |
| 9.00 | -10.70 | 61.8 | -39.16 | -144.4 | 17.19 | 56.4 | -4.90 | -53.3 |
| 10.00 | -8.32 | 24.9 | -37.57 | -170.5 | 17.48 | 20.2 | -5.99 | -56.8 |
| 11.00 | -7.00 | -1.8 | -36.41 | 168.3 | 17.54 | -10.5 | -7.27 | -59.4 |
| 12.00 | -6.48 | -23.4 | -35.43 | 149.3 | 17.55 | -38.0 | -8.87 | -60.5 |
| 13.00 | -6.63 | -42.1 | -34.71 | 131.5 | 17.53 | -63.6 | -10.85 | -57.5 |
| 14.00 | -7.33 | -58.2 | -34.27 | 114.2 | 17.44 | -88.2 | -12.73 | -46.1 |
| 15.00 | -8.51 | -71.5 | -34.16 | 98.4 | 17.23 | -112.3 | -13.16 | -27.4 |
| 16.00 | -9.93 | -79.7 | -34.42 | 83.4 | 16.85 | -135.9 | -11.71 | -13.0 |
| 17.00 | -11.00 | -82.6 | -35.18 | 70.8 | 16.29 | -158.6 | -9.84 | -8.5 |
| 18.00 | -11.11 | -83.8 | -36.29 | 61.5 | 15.59 | 179.4 | -8.29 | -9.4 |
| 19.00 | -10.35 | -88.5 | -37.52 | 58.2 | 14.75 | 158.2 | -7.17 | -13.1 |
| 20.00 | -9.53 | -100.1 | -38.26 | 59.5 | 13.82 | 137.2 | -6.34 | -18.1 |
| 21.00 | -8.97 | -117.1 | -37.98 | 64.4 | 12.71 | 115.9 | -5.86 | -23.7 |
| 22.00 | -9.04 | -137.0 | -36.56 | 64.7 | 11.36 | 95.5 | -5.47 | -29.3 |
| 23.00 | -9.70 | -161.0 | -35.28 | 56.8 | 9.72 | 75.4 | -5.35 | -34.7 |
| 24.00 | -10.97 | 174.2 | -34.49 | 47.1 | 7.77 | 56.6 | -5.37 | -39.3 |
| 25.00 | -12.61 | 144.5 | -34.15 | 36.2 | 5.59 | 39.2 | -5.41 | -43.4 |
| 26.00 | -14.42 | 110.6 | -34.37 | 24.8 | 3.10 | 23.8 | -5.70 | -46.2 |

Typical Results

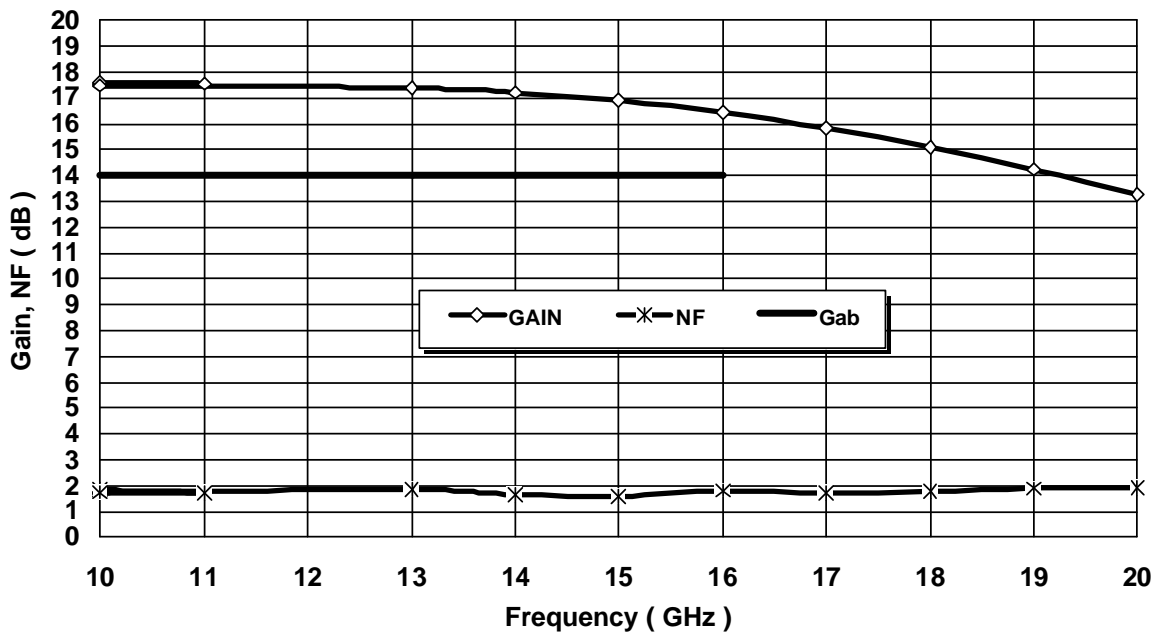
Chip Typical Response (On wafer Si) :

Tamb = +25°C

Vd = 4.0V ; Vg1 = Vg2 = +1.4Volt ; Id = 45mA (A,B,C,D & E not connected)



Typical Gain and Matching measurements on wafer.

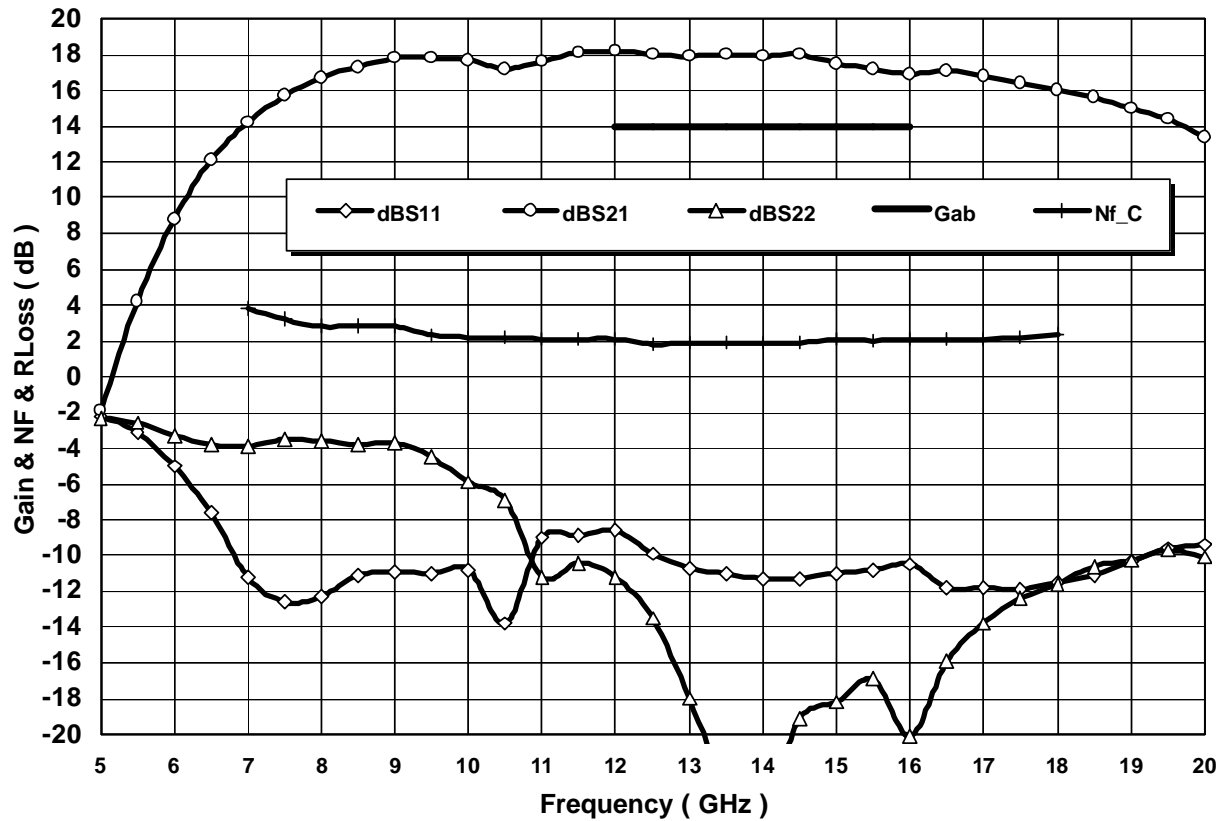


Typical Gain and Noise Figure measurements on wafer.

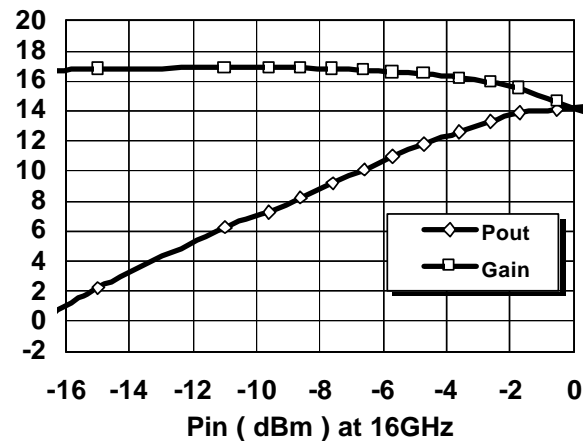
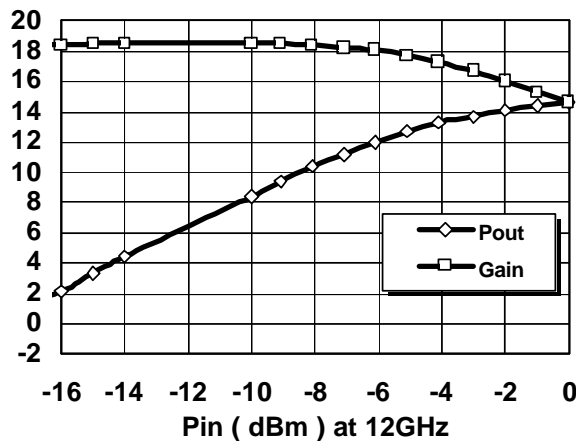
Typical Test-Jig Results

Circuit Typical Response (Test-Jig) :

Tamb = +25°C Vd = 4.0V ; B & E Pads grounded ; Id = 55mA (Vg1 & Vg2 NC)

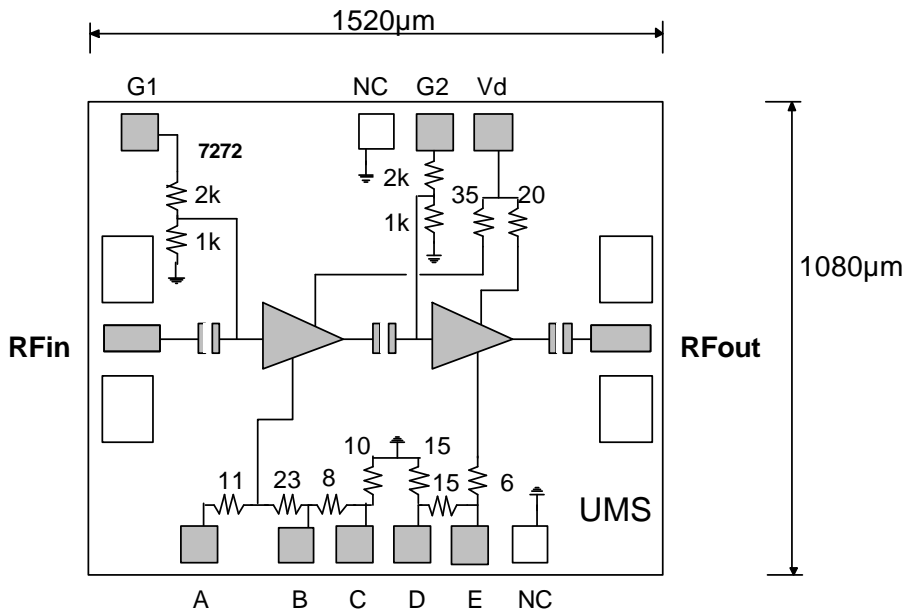


Typical Linear measurements in test-jig.

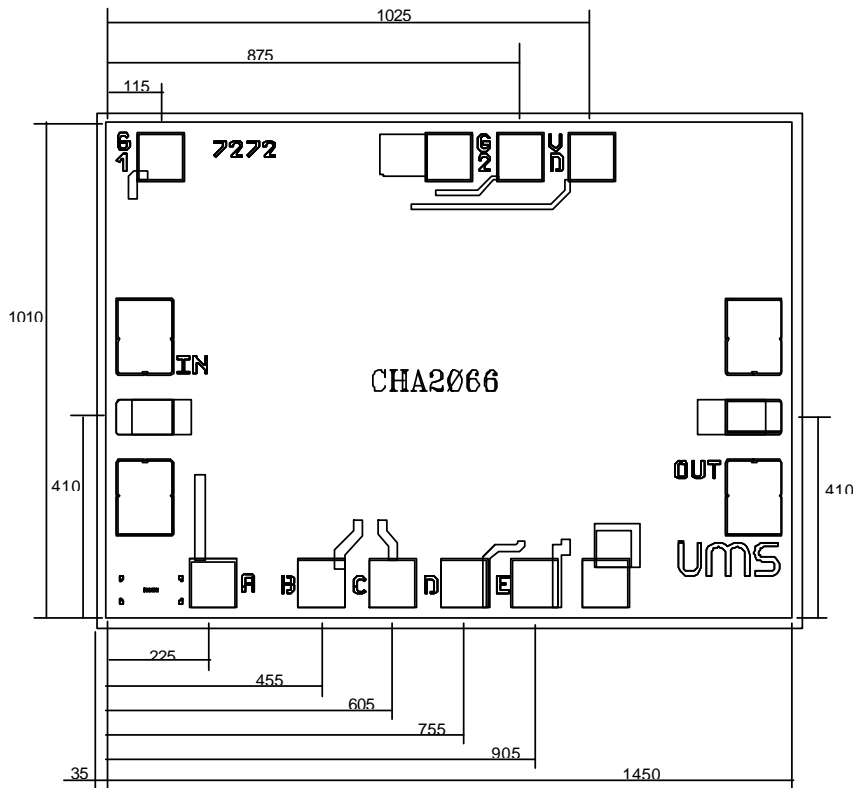


Typical Output Power measurements in test-jig.

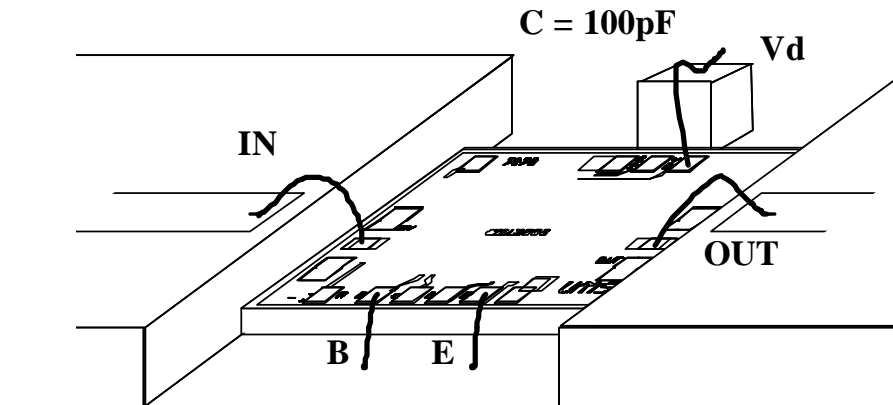
Chip schematic and Pad Identification



Pad size 100x100µm, chip thickness 100µm
 Dimensions : 1520 x 1080µm ± 35µm

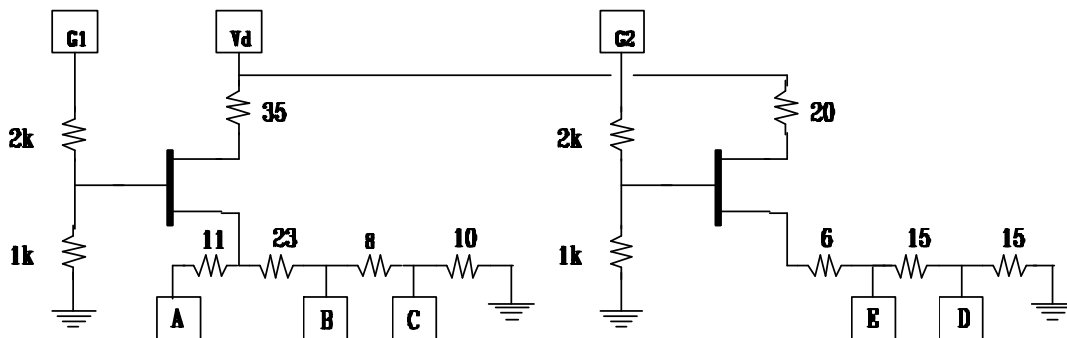


Typical Chip Assembly



Chip Biasing options

This chip is self-biased, and flexibility is provided by the access to number of pads. the internal DC electrical schematic is given in order to use these pads in a safe way.



The two requirements are :

N°1 : Not exceed $V_{ds} = 3.5\text{Volt}$ (internal Drain to Source voltage).

N°2 : Not biased in such a way that V_{gs} becomes positive.
(internal Gate to Source voltage)

We propose two standard biasing :

Low Noise and low consumption :

$V_d = 4\text{V}$ and B & D grounded.

All the other pads non connected (NC).

$I_{dd} = 45\text{mA}$ & $P_{out-1dB} = +10\text{dBm}$ Typical.

(Equivalent to A,B,C,D,E : NC and $V_d=4\text{V}$; $G1=+1.4\text{V}$; $G2=+1.4\text{V}$).

Low Noise and high output power : $V_d = 4\text{V}$ and B & E grounded.

All the other pads non connected (NC).

$I_{dd} = 55\text{mA}$ & $P_{out-1dB} = +13\text{dBm}$ Typical.

(Equivalent to A,B,C,D,E : NC and $V_d=5\text{V}$; $G1=+1.4\text{V}$; $G2=+4.0\text{V}$).

A file is available on request to help the biasing option tuning.

Ordering Information

Chip form : CHA2066-99F/00

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